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Attorney Docket No. TI-26904

Assistant Commissioner for Patents
Washington, D. C. 20231

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Transmitted herewith for filing is the patent application of:

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David W. West

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For: **DOUBLE SIDED FLEXIBLE CIRCUIT FOR INTEGRATED CIRCUIT PACKAGES AND METHOD OF MANUFACTURE.**
Enclosed are:

__7__ Sheets of formal drawings and __23__ pages of Specification (including Abstract)
__x__ A Declaration/Power of Attorney
__x__ Assignment with form PTO 1595

Please amend the specification by inserting before the first line the sentence:
This application claims priority under 35 USC § 119 based upon **Provisional Patent Application number 60/122,297, filed 03/01/99.**

FEE CALCULATION					FEE
	NUMBER		NUMBER EXTRA	RATE	BASIC FEE $ 690.00
Total Claims	20	-20 =	0	X $22 =	$0.00
Independent Claims	5	- 3 =	2	X $82 =	$164.00
				Total Filing Fee	$854.00

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All correspondence related to this application may be addressed to the undersigned at Navarro IP Law Group, P.C. 801 E. Campbell Rd. Suite 655, Richardson, TX 75081.

Date: February 28, 2000

Gary C. Honeycutt
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February 28, 2000

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Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Patent Application For:
DOUBLE SIDED FLEXIBLE CIRCUIT FOR INTEGRATED CIRCUIT PACKAGES AND METHOD OF MANUFACTURE.
Attorney Docket No. TI-26904
Our File: 1000-2104

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Sincerely,

Gary C. Honeycutt
Reg. No. 20,250

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DOUBLE SIDED FLEXIBLE CIRCUIT FOR INTEGRATED CIRCUIT PACKAGES AND METHOD OF MANUFACTURE

FIELD OF THE INVENTION

The present invention relates generally to flexible circuits and more particularly to a method of fabricating flexible circuits for integrated circuit package interconnections.

BRIEF DESCRIPTION OF RELATED ART

As the demand for cheaper, faster and lower power consuming integrated circuits increases, so must the packing density at the circuit board level. Not only have techniques continually evolved to meet the demand for minimizing dimensions of the transistors and of the electrical interconnections which integrate semiconductor devices, but also the packaging technology has advanced resulting in smaller integrated circuit packages with improved electrical and thermal performance.

Ball Grid Array (BGA) and many Chip Scale Packages (CSP) are integrated circuit packages which are assembled to an external circuit board using an array of solder balls confined within the area of the package. The solder balls are electrically connected to an external circuit board, and the external connections to the chip are made through conductive vias and conductor traces in the package substrate. An example of an area array package is shown in Figure 1a and is compared to a leaded package illustrated in Figure 1b. With area array packages, such as the CSP depicted in Figure 1a, solder balls external contacts 101 eliminate the protruding leads 121 of leaded packages in

Figure 1b, thereby providing a more compact package which requires less circuit board space. A printed circuit substrate 102 supports the die and provides electrical interconnection between the die and external contact solder balls. The printed circuit substrate replaces the die support pad 122 and the internal lead frame 123 of leaded packages in Figure 1b, allowing improved performance by lower inductance of the shorter interconnection between the chip and the external circuit board. An additional advantage of the printed circuit substrate is achieved by incorporating multiple common power and/or ground planes into the substrate.

Integrated circuit chips 104 are electrically connected to the interconnect circuitry on the substrate either by wire bonding or by flip chip 103 connections. Typical substrates are of rigid printed wiring board construction, or for more advanced small and closely spaced circuits, an unsupported flex circuit provides interconnections. Electrical connection between the printed circuitry 105 on the chip side of the substrate and the external contact solder balls is typically realized by conductive vias 106 through the substrate.

Printed circuits are typically fabricated by preparing by an enlarged-scale artwork master of a circuit pattern and conductor paths, and then the enlarged-scale artwork master is photographically reduced to the desired size. Screens and masks are fabricated according to the reduced circuit pattern for the application of photoresist materials. Processes including etching, screening, plating, laminating, vacuum deposition, via hole formation, and protective coating application are used to fabricated both supported printed circuits and unsupported flexible circuits.

Substrates for area array packages on flex circuits are most commonly fabricated on a dielectric polymer base film in reel or sheet format. A copper metal is applied to both surfaces of the dielectric film either by bonding a thin foil to the base film, or by vapor depositing the metal and subsequently plating to the necessary conductor thickness. Interconnect traces and contact pads are patterned and etched in the metal. Several techniques are known for electrically interconnecting the conductors and contacts on either side of the substrate. Vias are typically formed by mechanical punching or by laser ablation, and the vias are filled with a conductor by plating, by metal deposition during the film metallization, or by filling with conductive pastes. Completing the fabrication of a circuit includes plating a layer of nickel and a thin film of gold over the conductors for environmental protection, and to support solder contacts. A solder mask coating is applied to the circuitry on the surface to be soldered in order to control the solder run out.

All of these fabrication techniques require multiple plating and etching steps. In the case of laser ablation where one via is formed at a time, the process is repetitive and time consuming. Further, the existing techniques for making conductive vias suffer from difficulties in making the through holes consistently conductive, and in aligning the top and bottom circuits with the vias. Via conductivity failures occur either as electrical opens or as intermittent contacts resulting from separations in the thin conductor walls during thermal excursions due to expansion mismatch between the conductor and the substrate, from incompletely coating by vapor deposition, from air pockets entrapped in the vias during plating from both sides of the circuit, from fatigue failures of the thin conductors, from marginal

conductivity of the filling material, and/or from marginal contact due to misalignment of the circuit and vias.

It is accordingly desirable to provide a reliable flexible circuit substrate for integrated circuit area array packages, and a method of manufacture that permits high volume production without the reliability issues identified for current processes, and which eliminates the need for costly vapor deposition or multiple laser drilling.

SUMMARY OF THE INVENTION

The principal object of the present invention is to provide a reliable, double sided electrical interconnection flexible circuit which enables interconnecting integrated circuit chips to an external circuit, and a method of manufacturing the flex circuit. The preferred embodiment of the invention provides a flexible circuit substrate for area array packages including conductor patterns on the first surface of a flexible dielectric film which permit interconnection between the chip terminals and from the chip terminals to conductive vias through the dielectric film. It further includes, on the second surface a plurality of contact pads for attachment of solder balls for external contact to a second level of interconnection, and the conductors on the two surfaces are interconnected by reliable, solid metal conductive vias. The unique conductive vias comprise metal studs etched from a metal matrix, preferably comprising copper, and the studs when pressed through the dielectric film contact the conductive material on the first surface of the dielectric. The copper matrix with raised studs is attached to the second surface of the dielectric film, and the unraised portion of the matrix provides the pre-patterned solder ball contact pads.

The flex circuit of the present invention, therefore, includes a plurality of studs etched from a metal matrix with a which serve as both the tool to punch apertures for the vias, and to simultaneously fill the vias. The unraised film portion of the metal matrix provides the base metal which will subsequently be patterned to form the solder ball contacts, and thus the film and the studs become a part of the finished flex circuit.

It is further an object of the invention to provide a predecessor embossing tool for use of and inclusion into the flexible circuit, and a method of manufacturing the tool. The embossing tool comprises a copper matrix etched to form raised studs corresponding to a pattern of conductive vias in a flexible circuit. The etched studs of the copper embossing tool when adhered to the base dielectric film, and a hydraulic force applied, punch a plurality of cylindrical apertures in the film, and simultaneously fill the apertures. When pushed through the dielectric, the studs contact conductors on the opposite surface of to solid conductive vias through the dielectric.

To complete the fabrication of the intermediate base structure for a flex film, additional copper is electroplated onto the surfaces to both increase the conductor thickness, and to seal the connection between the solid Cu via and the copper film on the first surface, thereby insuring robust electrical contact. Subsequently, the copper on both surfaces is photopatterned and etched to provide interconnections and bump solder pads. The patterns on either side are aligned to the vias, thereby eliminating the problems associated with aligning patterns on opposite sides of a film.

It is further an object of the invention to provide a method for fabricating a flex circuit substrate which has high yield, low cost, and is amenable to mass production. In addition to the etched metal matrix, a die set precisely matched to the etched studs facilitates punching apertures for vias in the film. Reel to reel processing and transport are the preferred techniques for fabrication of substrates which may then be assembled into packages using the same format. However, the processes are not limited to this technique, nor is the specific flex circuit application.

In an alternate embodiment, a metal embossing tool is coated in the selective raised areas with a thin film of copper which under temperature and pressure adheres to the dielectric film simultaneously with the embossing process. The embossing tool is removed, leaving depressed interconnect patterns, contact pads and/or vias coated with copper. The exposed copper is subsequently plated with copper. The process eliminates patterning and etching in the manufacture of a flex circuit, as well as the need for a solder mask on solder ball contact surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a is an example of an area array chip sized package with flex circuit substrate. (Prior art)

Figure 1b shows an example of a leaded package with lead frame. (Prior art)

Figure 2a is a cross sectional view of a flex circuit of the present invention.

Figure 2b shows an array of solder bump contact pads and vias of the present invention.

Figure 2c provides an example of contact pads from chip terminals, interconnection patterns and vias of the present invention.

Figures 3a-3d are illustrations of fabrication steps for an etched metal matrix for subsequent flex circuit application.

Figures 4a - 4e illustrate the fabrication steps for forming vias in a flex circuit using an etched metal matrix.

Figures 5a- 5c show the plating process steps for fabricating a flex circuit with an etched metal matrix in place.

Figure 6 demonstrates a die tool set to facilitate aperture punching.

Figure 7 shows the surface of an embossing tool with thin film copper coating on the raised areas.

Figure 8 shows the depressed and metallized solder ball contact pads, vias and interconnections to vias.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with the preferred embodiment of the current invention, a double sided flexible interconnection circuit 200 for use as an integrated package substrate is shown in cross-sectional view in Figure 2a. The flex circuit includes a base dielectric film 201 of a flexible polymer patterned on the first surface 201a with interconnection traces 202 from the chip terminal pads to conductive vias 203, which provide electrical contact to solder bump contact pads 204 on the second surface 201b of the dielectric film.

A typical pattern of solder ball contact pads 204 for a flex circuit package substrate is shown in Figure 2b. The pads 204 on the second surface 201b of the dielectric film are arrayed in a pattern which will align to and allow contact to be made by solder balls (not shown) to a printed wiring board, or other second level of interconnection. As shown in both Figures 2a and 2b, the contact pads 204 are interconnected to the conductive vias 203 by metal traces 205, or the pads coincide with and overlap the conductive vias.

Figure 2c provides a section of an exemplary interconnection pattern on the first surface 201a of a flex circuit. A plurality of contact pads 211 for bond wires or flip chip bumps from the chip are interconnected by conductor traces 210 from the pads 211 to vias 203, and/or to shared traces 212 between chip contacts pads, such as for a power or ground bus with multiple contacts by the chip.

A plurality of solid metal conductive vias 203 electrically connect the patterned conductors on each surface of the dielectric film. The conductive vias of the preferred embodiment of the current invention comprise metallic studs etched from a metal matrix. The studs are

attached to an unraised portion of the metal matrix on the second surface 201a of the flex circuit. The metal film matrix adhered to the dielectric flex film provides the base metal of the solder ball contact pad 204. The metal matrix with etched studs comprises copper.

An etched metal stud 203 contacts the interconnection pattern 202 on the first surface 201b of the dielectric film, and is intimately attached to the base copper metal of the solder ball contact pad 204 on the second surface 201a of the dielectric film 210, thereby forming a the solid metal conductor via 203. Reliability of the copper stud contact to the conductor pattern on both surfaces of the dielectric film is insured by a layer of plated copper 206 to fill any voids at the interfaces.

The device of this invention has been described wherein the metal matrix with raised studs is a portion of the solder ball pads on the second surface of the dielectric film. In an alternate embodiment, the surfaces are reversed and the metal matrix with studs forms the base metal layer of the interconnect pattern or first surface of the dielectric film, and the copper studs engage with the solder ball contact pads on the second surface.

Interconnection circuitry on the flex circuit substrate further includes a thin film of nickel and gold over the exposed copper patterns to provide environmental protection and a bondable surface. A solder mask surrounds the solder ball pads on the second surface to complete the patterned area of the flex circuit.

The preferred embodiment has been described as a flexible circuit which constitutes the major component and interconnection for an integrated circuit substrate, however, it is not limited to this application, but is

intended to cover flexible circuits having interconnections on two sides.

Turning now to a method of fabricating the flex circuit of the current invention having a plurality of conductive vias comprising the etched studs of a metal matrix which serve to electrically interconnect the circuitry on the two surfaces of the flex film substrate. It is necessary to fabricate a metal matrix having raised studs corresponding to a pattern of vias for a specified flex circuit. The matrix with raised studs constitutes the tool used to punch the apertures for vias, to fill the vias with the studs, and to provide the base metal for the solder ball contact pads on the second surface of the dielectric film.

Figures 3a through 3d illustrate cross sectional views of a the process steps for forming a metal matrix tool to be used subsequently to fabricate a flex circuit. A strip of a conductive metal 301, preferably comprising copper, in the range of 0.003 to 0.006 inches in thickness is coated with a photoresist 310 on both major surfaces, as shown in Figure 3a. A plurality of photoimaged via sites 302 are developed on the first surface 301a in a conventional manner, i.e., artwork is placed over the photoresist and the photoresist is exposed using a high intensity UV light source. As seen in Figure 3b, the photoimaged via sites 302 on the first surface 301a are protected by photoresist 310 and the exposed metal is partially etched in Figure 3c using a commercially available ammoniacal copper etchant. The photoresist is then removed using a commercially available stripping solution, leaving a copper film 311 with a plurality of etched studs 315, as shown in Figure 3d wherein the transverse studs 315 correspond to the via pattern for a flex circuit substrate. The metal matrix after etching is in the range of 0.00075 to 0.0015 inches thick in the etched

areas 311 and in the range of 0.003 to 0.006 inches in the protected areas. The raised, unetched areas of metal are used as studs 315 in the flex circuit fabrication. Height of the studs will be selected as a function of the thickness of the flex circuit substrate; i.e., the studs must be of sufficient height to completely pierce the flex film.

A reverse image of the photomask for the embossing tool is used to fabricate a die plate precisely matched to the vias. The die plate provides an opening through which residue from the punching operation will be extruded; this will be discussed later under the subject of mechanization.

Figures 4a through 4d illustrate the steps to form solid vias for a flex circuit using the etched metal matrix 305 fabricated in Figures 3a through 3d. In Figure4a, a commercially available dielectric film 402, such as a polyimide polymer in the range of 0.003 to 0.006 inches thick having an unpatterned copper layer 403 attached to first surface 404 is the base material for a flex circuit of the current invention. The copper layer is in the range of 0.0005 to 0.0015 inches thickness. The second major surface 406 of the dielectric film is cleaned, and with a heat activated adhesive material 416.

In Figure 4b, the copper matrix 311 with etched studs 315 is positioned on the adhesive coated second surface 406 of the dielectric film 402. The copper film matrix and studs are selected so that the height of the studs 315 are equal to, or greater than the thickness of the dilectric film 402 with associated copper film 403.

In Figure 4c, the assemblage from Figure 4b is positioned in a hydraulic press and pressure as indicated by arrows 420 is applied to said assemblage, whereby the solid copper studs 315 force a plurality of cylindrical apertures in the dielectric film 402 and associated copper layer 403.

The material extruded from the film by the studs is represented as compressed dielectric layer 402b and copper 403b.

The apertures are filled by the copper studs 315 simultaneously with the punching to forming a plurality of solid copper vias in the dielectric film 402. Within the same process, the copper matrix film 311 contacts the adhesive material 416 on the second surface 406 of the dielectric film. In Figure 4d, the assemblage is passed through a heated press to insure adhesion of the copper matrix 311 to the adhesive 416 coated second surface 406 of the dielectric film.

The vertical surfaces of the copper studs 315 of the studs opposite the film matrix 311 terminate in contact with the copper layer 403 on the first surface of the dielectric. The copper stud 315 and the copper layer 403 are press fit forming an intact solid copper layer 408 on the second surface of the flex film.

In Figure 5a the flex film 402 with copper layer 408 and the copper matrix film 403 on one surface, and copper matrix 311 on the opposite surface are passed through a copper electroplating step wherein a thin film of plated copper 509 is deposited over the exposed copper layers. The plated copper 509 insures a reliable layer of copper and fills any defects from processing or mating of layers. Conventional electroplating processes of cleaning, surface activation, plating, rinsing and drying are used to plate the copper layers 509 on the existing copper layers. These steps have formed an intermediate base structure for a flex circuit, having solid metal vias attached to a copper layer on both surfaces.

The process steps illustrated in Figures 4a through 4d result in a copper clad flexible dielectric film including a

plurality of solid metal filled conductive vias in an array corresponding to the via conductor paths through a circuit pattern for an integrated circuit package for ball grid array or chip scale package substrate. The additional copper plated layer 509 insures a uniform, void free copper surfaces. The simple, one step punch and fill vias from an etched metal matrix replaces the costly, multistep laser ablation, cleaning, metal vapor deposition and plating filling of exiting technology, and further results in a robust self-aligned connection between the conductor surfaces.

Figures 5b through 5d illustrate the near conventional steps to complete fabrication of a flex circuit substrate using the dielectric film 402 with copper layers 408/509 on the first surface and layers 311/509 on the second surface, and with conductive vias 315 as produced in Figures 4a through 4d. In Figure 5b, conventional processes are used to laminate a photosensitive film 515 to the first surface of the via filled film, and a circuit interconnection photomask is aligned to the vias, and exposed by a strong UV light source. A second photoresist layer 516 is laminated to the second surface, a photo pattern for the solder ball contact pads is aligned to the vias, and exposed. The photoresist patterns on both sides are developed and the exposed copper films are etched to form the substrate patterns as demonstrated in Figure 5c using the patterned photoresist to protect the copper of the circuit pattern 502, the solder ball pads 504 and the underlying vias 315 during copper etching.

The photoresist is removed by conventional stripping methods and in Figure 5d, the metal patterned surfaces are plated first with nickel 512 and with gold 513 to protect against environmental and chemical attack. A solder mask 514

is applied to the solder ball contact pad surface surrounding each of the metal pads.

Processes and material required for completing the metallization overlying the patterned copper circuits are typical of those used for flex circuit formation, except that alignment of the patterns is specifically to filled vias, as opposed to some existing technology wherein the surfaces are patterned and subsequently vias formed which must align to and connect the patterns on both surfaces.

Mechanization for fabricating a flexible circuit for use as an integrated circuit area array package substrate is well adapted to reel to reel film transport. The appropriate film width will be selected for single or multiple packages, as required by the end user transport equipment. Continuous processing to form an intermediate structure for a flex circuit includes the following steps: alignment of a metal matrix having etched studs to a dielectric film, and to a die plate having apertures specifically matched to the vias, compressing the matrix and film, heating to adhere the matrix to a heat sensitive adhesive and plating the copper coated structure. Further, continuous processing to pattern the circuit includes the steps of photolithography, copper etching, and electroless plating the patterns.

Figure 6 provides a schematic of an assemblage wherein a die plate 610 precisely matched to the studs 315 is positioned atop a second die plate 620 having larger openings, and constructed from a stiffer material to withstand repeated application of pressure. The tooling assemblage is housed inside a hydraulic press. The dielectric film with copper studs and surfaces is positioned atop the die press, studs 315 aligned to the first die plate 610 and pressure applied. As pressure is applied, apertures in the dielectric film 402 and copper layer 403 are punched

by the embossed studs 315, through the openings in the die plate, while the film structure is supported by the die plates 610 and 620. The residue from the formation of apertures in the film is ejected through the larger openings at points 621.

The film with assembled metal matrix is subsequently transported to a position in the press having a solid plate wherein the film assemblage is heated and compressed, which enables the copper studs to be press fit against the copper film on the second surface and against the walls of the dielectric film, as shown in Figure 4d. Reel to reel mechanization facilitates photolithography, etching and plating processes as required for the flex circuit production.

An alternate technique for fabricating the conductor patterns and vias of a flex circuit package substrate using an embossing tool includes the following steps. Securing a metal matrix with embossed studs and/or conductor patterns fabricated from known technology such as electroforming or etching, coating the raised areas with a loosely held thin film of copper, transferring the copper film to a dielectric film using heat and pressure, physically removing the matrix, and subsequently plating the appropriate thickness of copper over the thin film of copper. The process is repeated on the second surface having a pattern of solder ball contact pads aligned to the preformed vias. The embossed film is plating with copper from both sides, using the transferred metal as the seed layer.

Schematic drawings of the tools for side one is given in Figure 7. In Figure 7, raised areas for the conductor pattern 701, the via punches 702 and pad sites 703 are coated with a thin layer of copper. The base material 700 of the embossing tool is a metallic film. In similar manner,

an embossing tool for the second side of the flex circuit includes raised the solder ball contact pads, interconnections to vias and vias coated with a thin film of copper.

The copper film is selectively applied to raised portions 701, 702, and 703 of the tool from a copper powder in suspension adhering to thermoplastic adhesive on the tool, or by use of an embossing tool comprising iron, permanently masking the area where no copper is desired and plating a film of copper on the raised portions.

Figure 8 depicts the dielectric second surface of the flex circuit 800 with depressed solder ball contact pads 804 and interconnections 805 to some vias 806 resulting from embossing the dielectric film, coating the recesses with a thin film of loosely held copper, and subsequently plating copper onto the "seed copper. The dielectric serves the purpose of a solder mask between the contact pads and eliminates the need for this material.

Similar mechanization facilitates the embossing process for this transfer method as the preferred embodiment described earlier; i.e. reel to reel processing with heated press to effect the embossing procedure.

Advantages of the emboss and transfer method are that no etching or photolithography are required in the flex circuit process itself and that the conductor and contact pads are recessed into the dielectric film.

While the invention has been described in connection with preferred embodiments, it is not intended to limit the scope to a particular form set forth, but on the contrary, it is intended to cover alternatives, modifications and equivalents as may be included within the spirit of the invention and the scope of the invention as defined by the appended claims.

What is claimed is:

1. A double sided electrical interconnection flexible circuit, to enable interconnecting an integrated circuit chip to an external circuit, including:

a base dielectric film of a flexible polymeric material,

a conductor pattern on the first surface of dielectric film having a plurality of contact pads for interconnection from the chip terminals, interconnection between said pads, and from said pads to conductive vias through the film,

a plurality of solder ball contact pads on the second surface of the dielectric film patterned from an etched metal film matrix, and

a plurality of conductive vias, comprising metal studs etched from said metal matrix, which interconnect the conductors on the first surface to those on the second surface of said dielectric film.

2. The flexible circuit as described in claim 1 in wherein the metal matrix with etched studs comprise copper.

3. The flexible circuit as described in claim 1 wherein the etched studs everted from the metal matrix constitute a tool for punching a pattern of apertures corresponding to conductive vias in the dielectric film.

4. The flexible circuit as described in claim 1 which provides the interconnection circuitry for the substrate of an area array integrated circuit package.

5. The flexible circuit as described in claim 1 further including a plated copper layer disposed over the interconnect patterns and solder ball contact pads.

6. A flexible circuit as described in claim 5 which further including a plated layer of nickel and of gold over the conductor patterns and solder ball contact pads.

7. A flexible circuit as described in claim 1 further including a plurality of openings parallel to the film edges which correspond to a sprocket transport mechanism.

8. A flexible circuit as described in claim 1 wherein said base dielectric film comprises a polyimide polymer in the range of 0.003 to 0.006 inches thick.

9. A double sided electrical interconnection flexible circuit substrate for an area array integrated circuit package to enable interconnecting an integrated circuit chip to an external circuit including :

a base dielectric film of a flexible polymeric material in the range of 0.003 to 0.006 inches thick,

a conductor pattern comprising copper on the first surface of dielectric film having a plurality of contact pads for interconnection from the chip terminals, interconnection between said pads, and from said pads to conductive vias through the film,

a plurality of solder ball contact pads on the second surface of the dielectric film patterned from an etched metal matrix,

a plurality of solid conductive vias filled with metal studs comprising copper, etched from said metal matrix which interconnect the conductors on the first surface to those on the second surface of said dielectric film, and which constitute a tool for punching apertures in a pattern of conductive vias, and

a layer of plated copper disposed over said interconnect patterns and solder ball contacts, and a layer of nickel and gold over the plated copper.

10. A metal matrix embossing tool, comprising a copper film having a plurality of transverse studs.

11. A device as in claim 10 whereby said studs are punch tools for forming apertures in a dielectric film.

12. A device as in claim 11 whereby said studs are equal to or slightly greater in height than the dielectric film for a flexible circuit.

13. A device as in claim 12 whereby each stud on the embossing tool is adapted to simultaneously punch and fill the vias.

14. A device as in claim 10 wherein the unraised portion of the matrix adhered to the dielectric film and attached to the studs constitutes the base metal of a plurality of solder ball contact pads for a flexible circuit.

15. A method of manufacturing the metal matrix embossing tool as described in claim 12 including the steps of:

a. laminating a photoresist on each major surface of a metal matrix, comprising copper in the range of 0.003 to 0.006 inches thick,

b. aligning a photomask pattern corresponding to conductive vias in a flexible circuit to the first surface, exposing both surfaces with a strong uv lamp, and developing the unexposed resist,

c. etching the exposed copper to a thickness of about 0.0005 to 0.0015 inches in the etched area.

16. A method of manufacturing an intermediate base structure for a flex circuit including the steps of:

a. forming a plurality of apertures corresponding to a pattern of conductive vias in a flexible base polymer film having a layer of copper on the first surface by mating a metal matrix embossing tool as described in claim 10 to the second surface,

b. applying a force to said metal matrix so that the studs of the tool punch through the copper coated polymer film, thereby creating a plurality of vias filled with the studs, and attaching the film matrix to the second side of the flex film,

c. electroplating a thin film of copper onto both sides of the copper clad flex film.

17. A die plate mechanism, to facilitate punching apertures in a flex circuit film using studs etched from a metal matrix, including a relatively thin metal plate in the range of 0.004 to 0.010 inches thick having apertures precisely matched to said studs, and a relatively thick plate having larger apertures.

18. A method of manufacturing a flex circuit on a flexible base polymer including the steps of:

a. superimposing an embossing tool having a pattern of conductors and vias corresponding to a circuit design, wherein said raised areas are coated with a thin layer of metal, comprising copper,

b. applying heat and pressure to simultaneously emboss the film and to transfer said thin metal layer from the embossing tool to the dielectric film,

b. removing the embossing tool,

c. embossing a pattern corresponding to that of the second surface of a flex circuit, and simultaneously transferring a thin layer of metal into the embossed pattern,

d. physically removing the embossing tool,

e. plating a layer of copper to fill the vias and conductor patterns on both sides of the film, and

f. plating a layer of nickel and gold onto the exposed copper patterns.

g. applying a solder mask on the surface of the film surrounding the solder ball contact pads.

19. A method of making an embossing tool as in claim 18 wherein a thin layer of loosely held copper is selectively coated onto the raised areas of said tool by treating the raised areas with a thermoplastic adhesive and exposing to a suspension of copper powder.

20. An embossing tool, as in claim 18 wherein a thin layer of loosely held copper is selectively plated onto the raised areas of said tool.

ABSTRACT

A double-sides electrical interconnection flexible circuit particularly useful as a substrate for an area array integrated circuit package is described. A circuit having interconnection patterns on one surface and solder ball contact pads on the second surface are interconnected by solid copper vias formed from an array of raised studs etched from a metal matrix. In reel to reel format, the etched metal matrix is adhered to one surface of the film and forms the base metal for the solder ball contact pads. The matrix with studs are presses through the dielectric film with a copper layer on the opposite surface, thereby forming an intermediate structure for a flex circuit with self-aligned solid copper vias in a one step process. The contacts are reinforced by plating both surfaces with a layer of copper, and conventional processes are used to complete the circuit patterning.

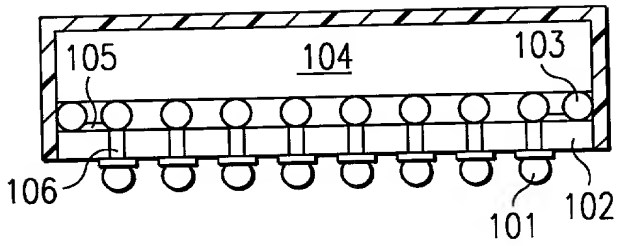


FIG. 1a

FIG. 1b

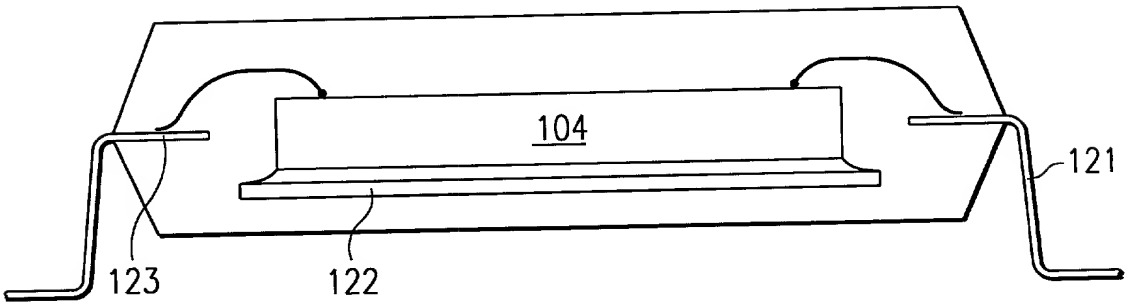
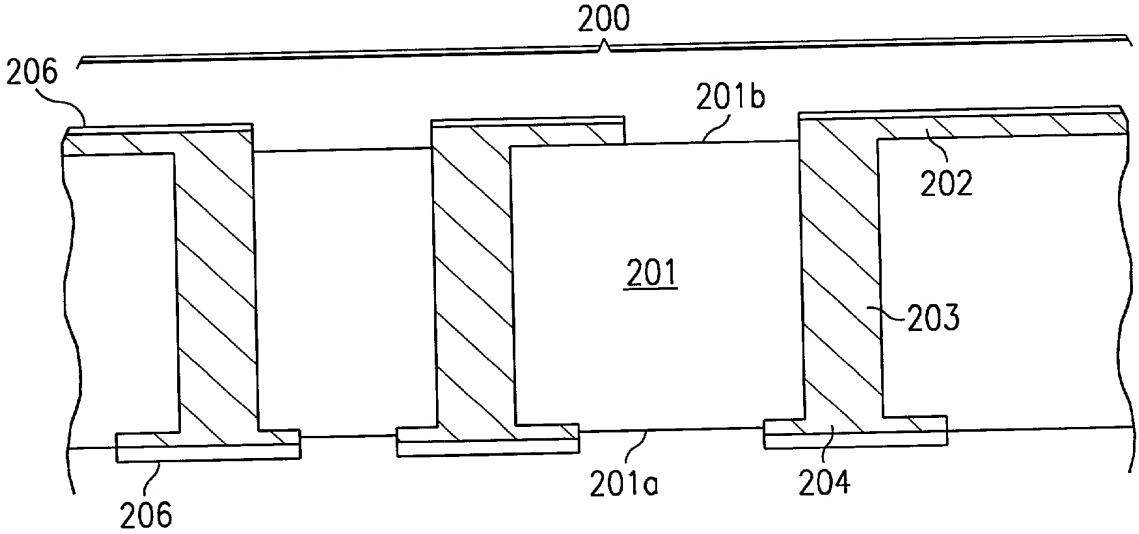


FIG. 2a



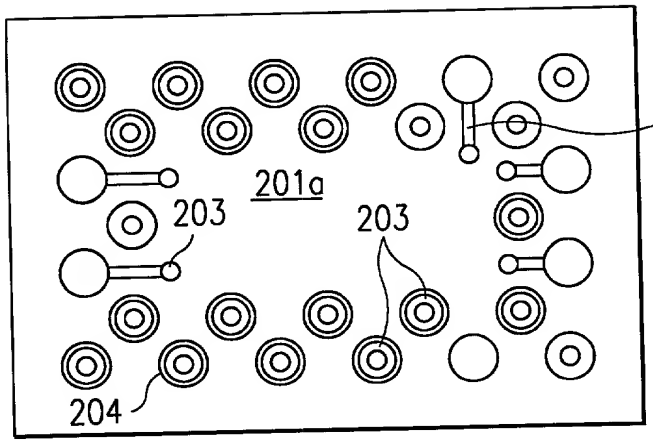


FIG. 2b

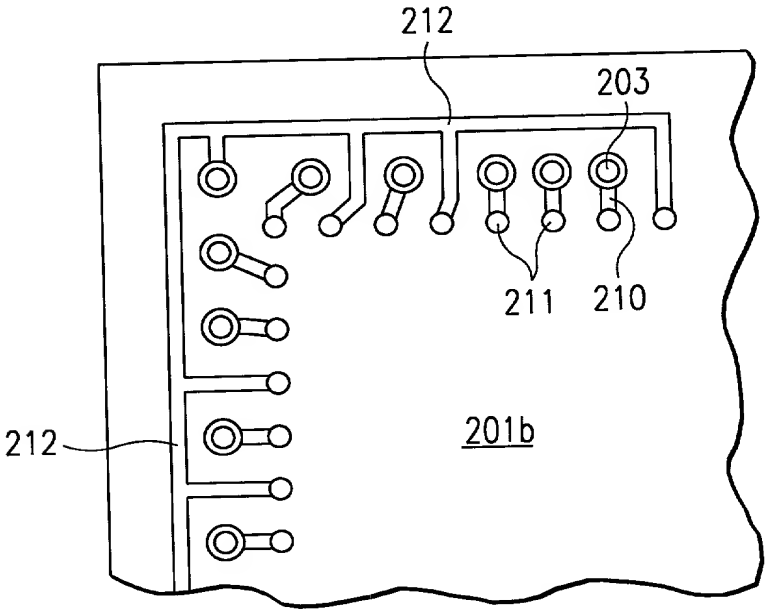


FIG. 2c

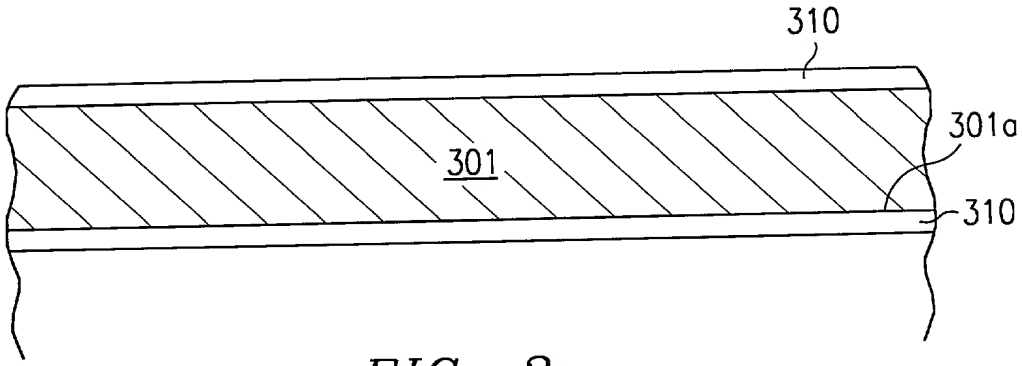


FIG. 3a

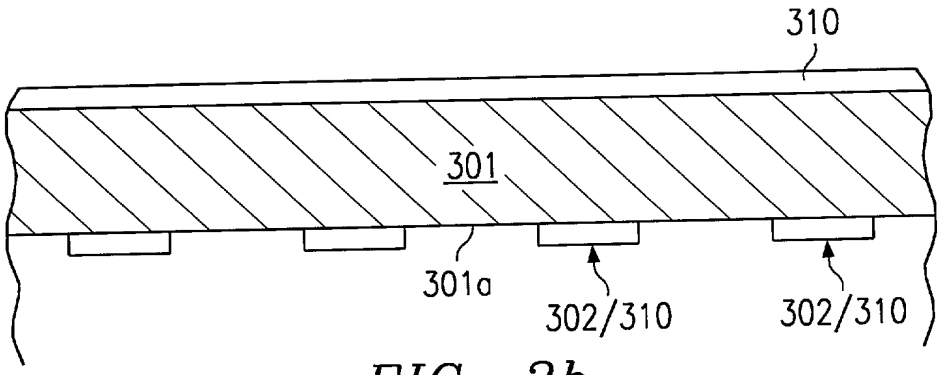


FIG. 3b

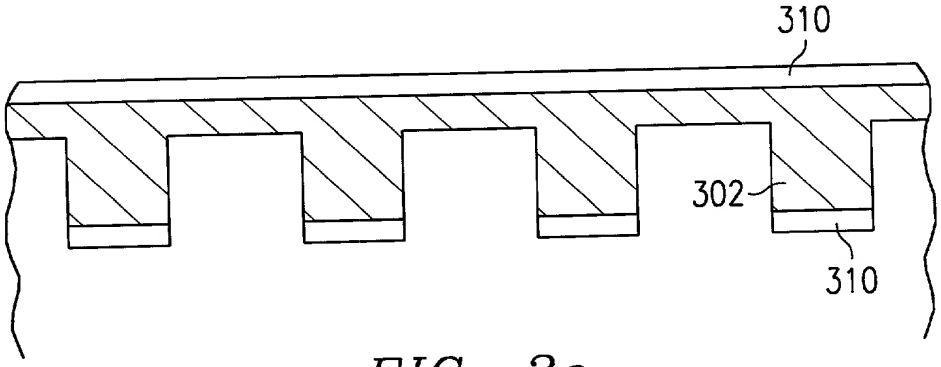


FIG. 3c

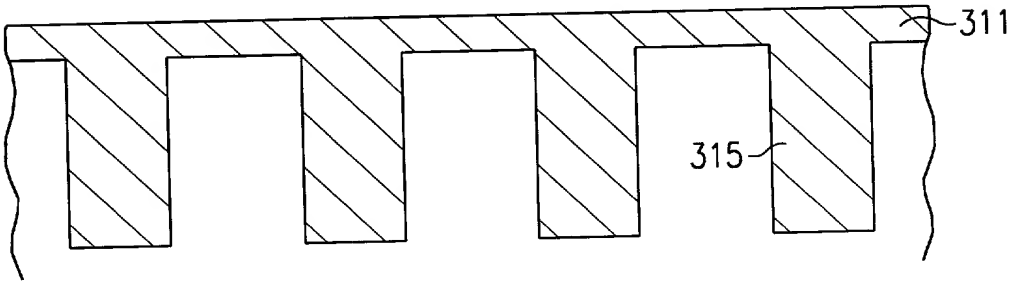


FIG. 3d

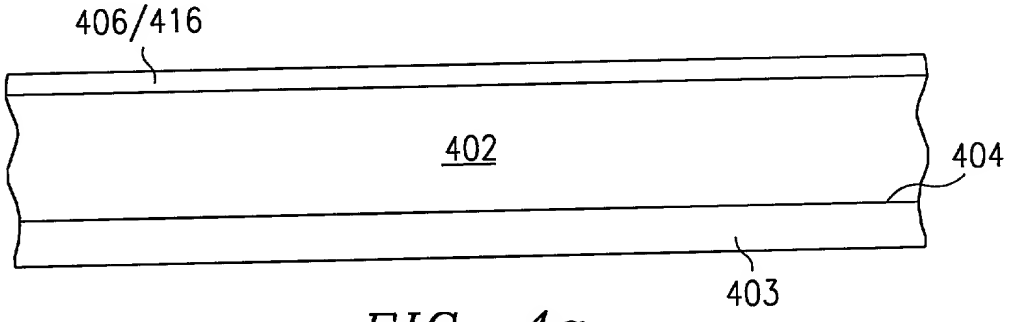


FIG. 4a

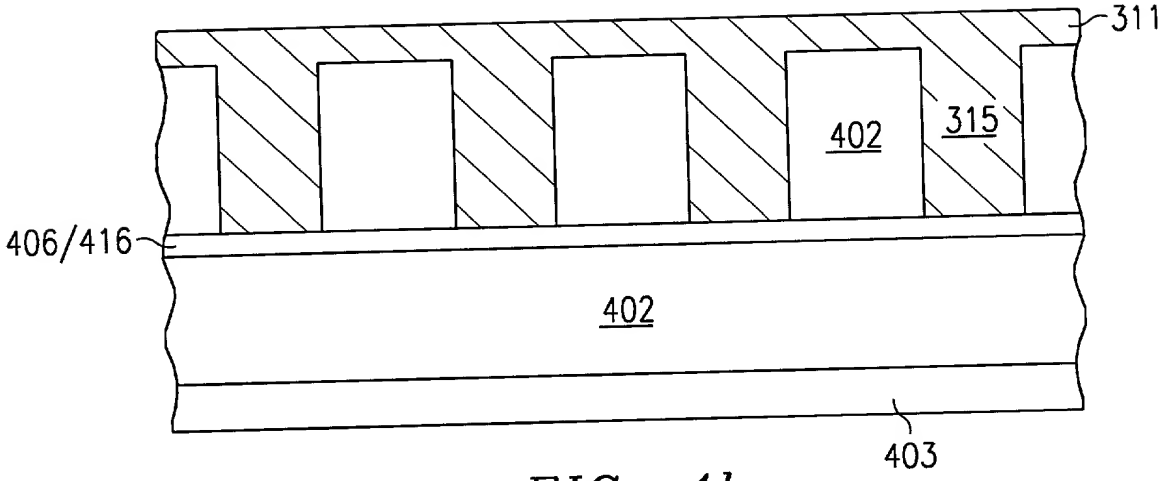


FIG. 4b

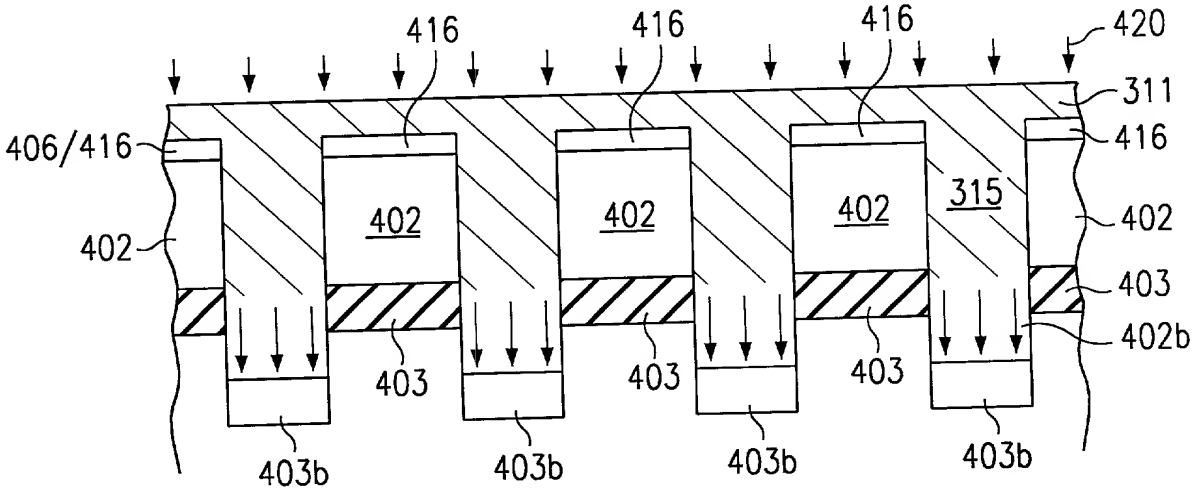


FIG. 4c

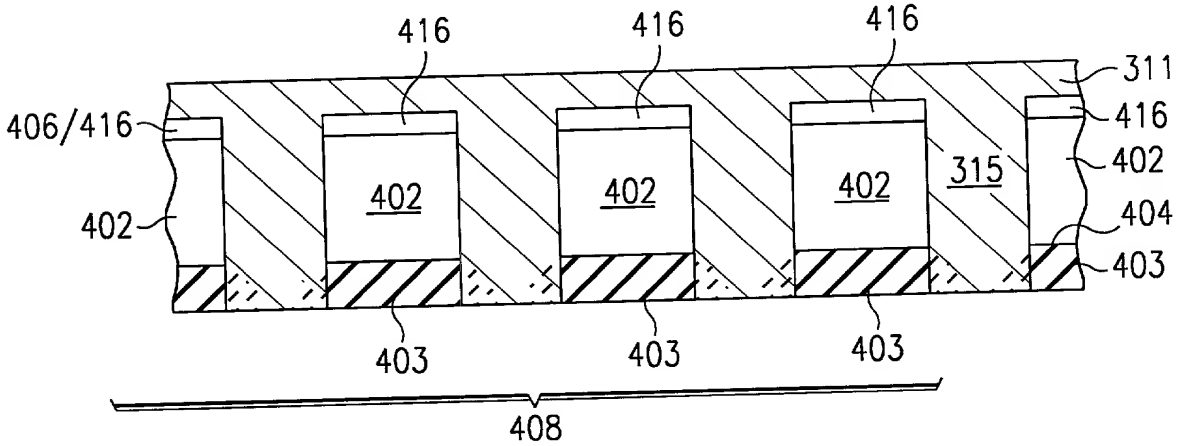


FIG. 4d

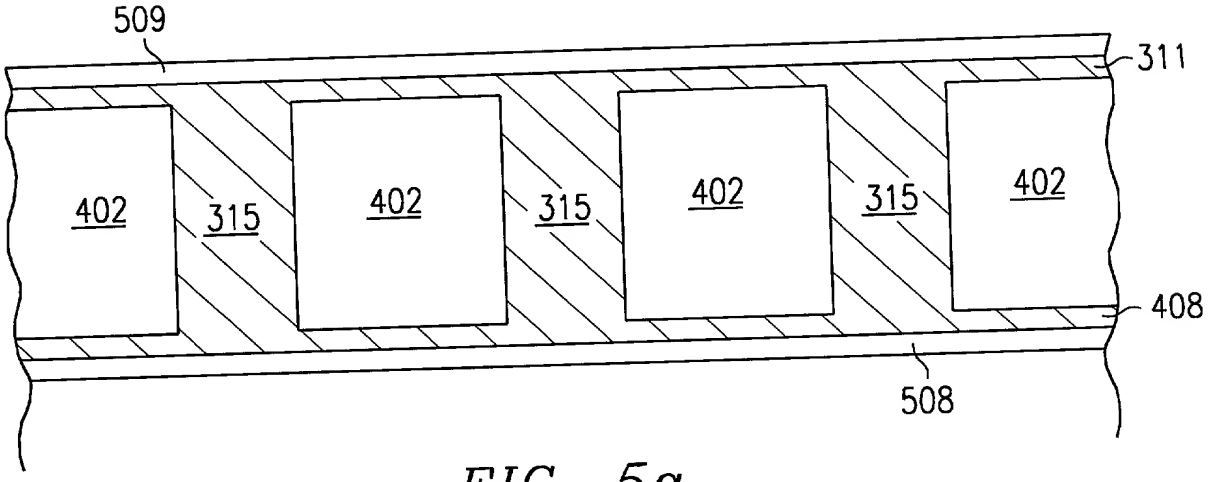


FIG. 5a

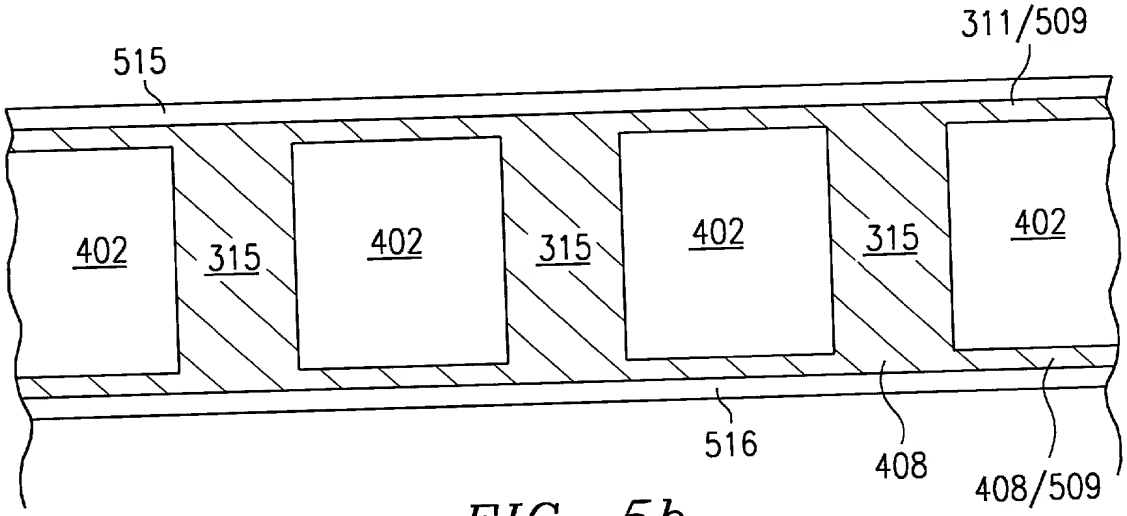


FIG. 5b

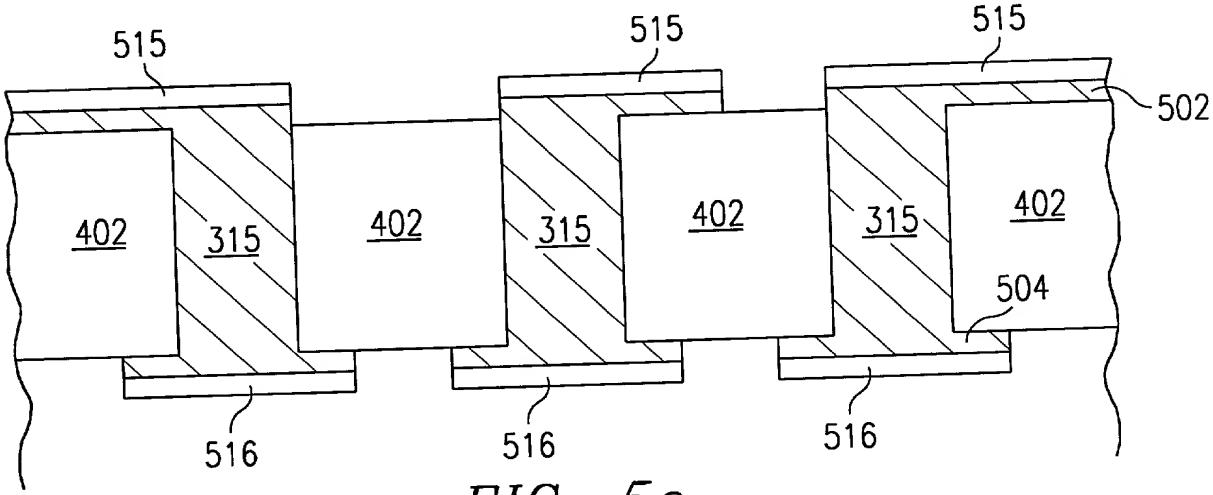


FIG. 5c

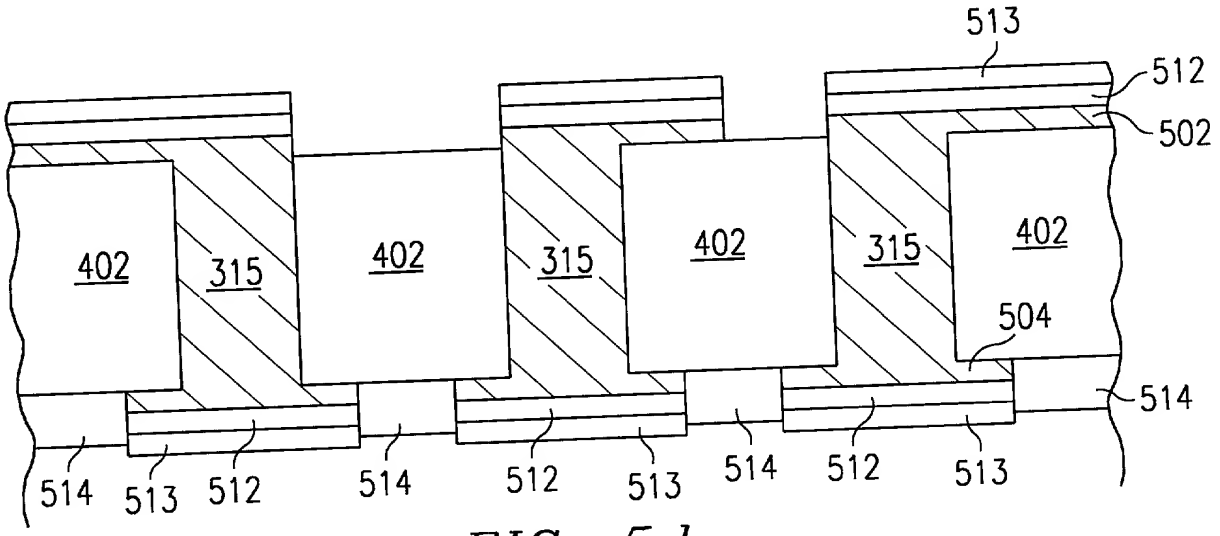

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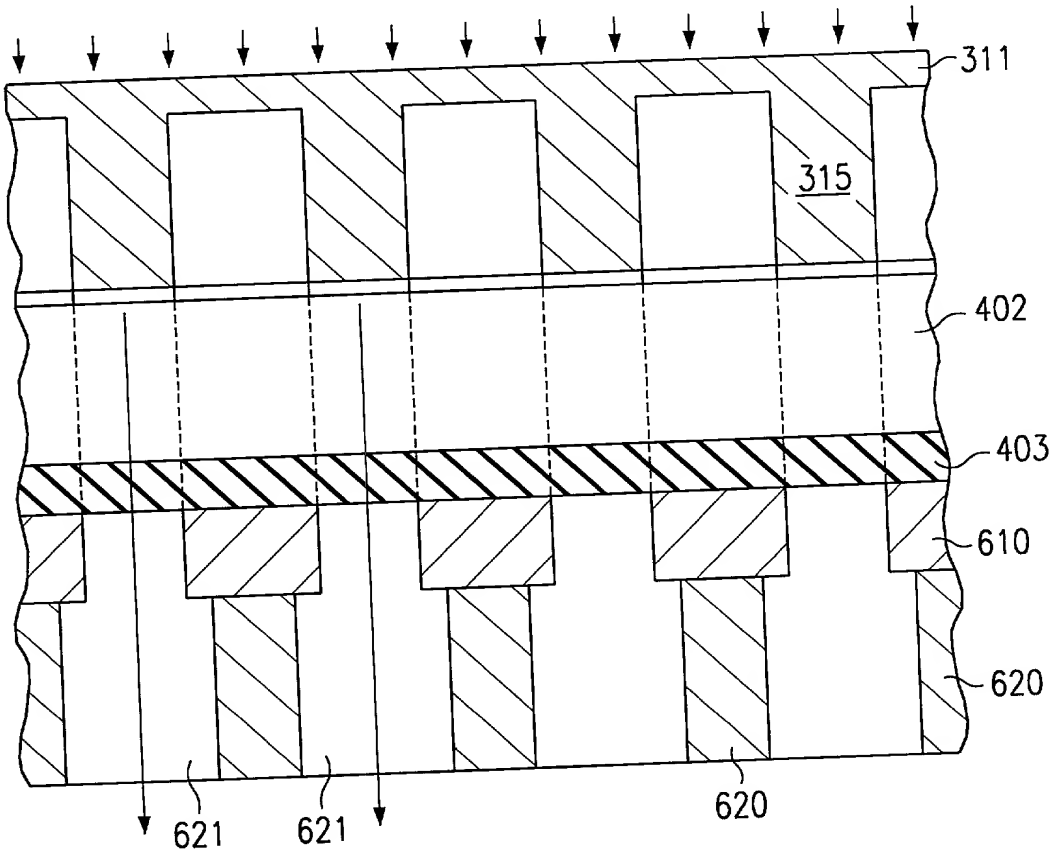
FIG. 5d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620

FIG. 6

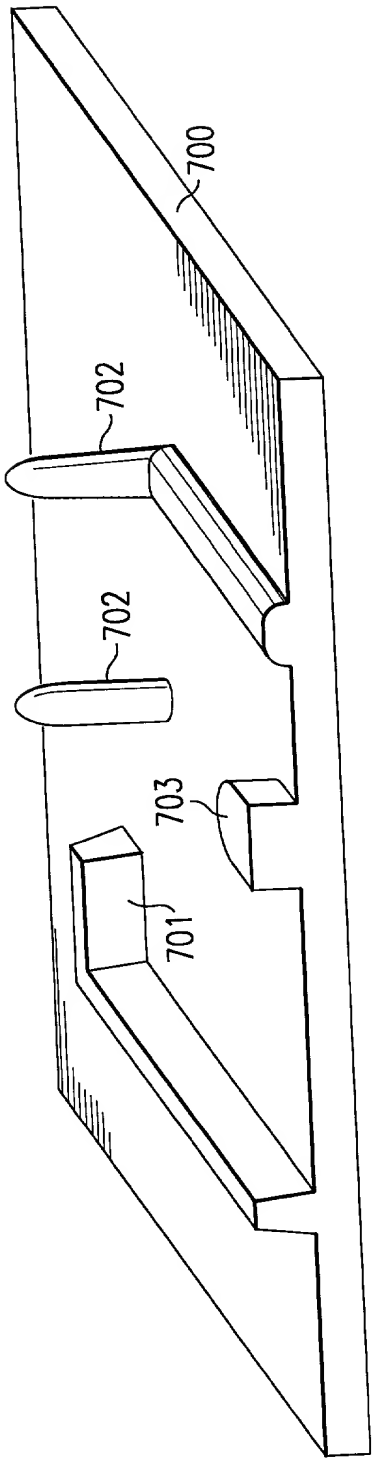

FIG. 7

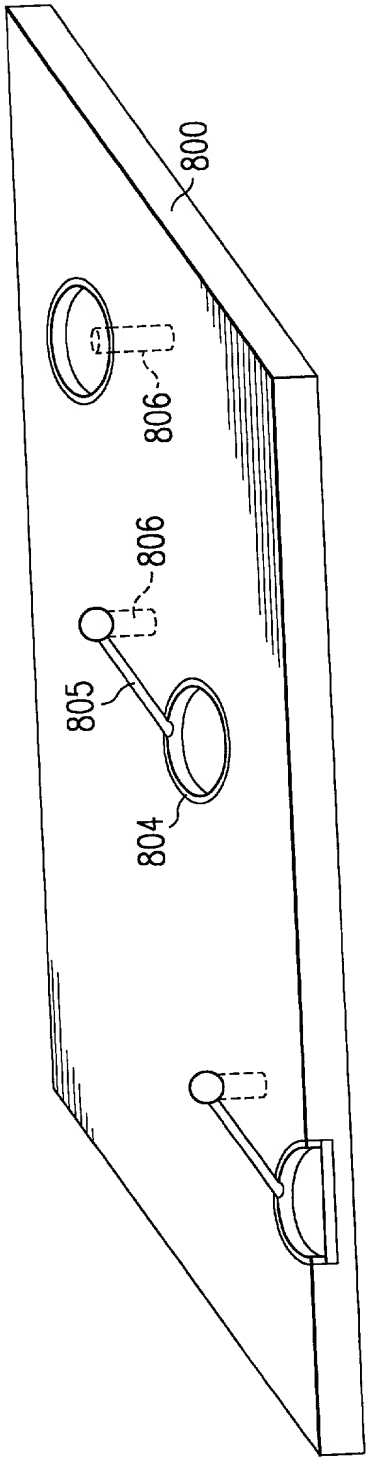

FIG. 8

ATTORNEY'S DOCKET NO.
TI-26904

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

Double Sided Flexible Circuit for Integrated Circuit Packages and Method of Manufacture

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Richard L. Donaldson, #25,673; Jay M. Cantor, #19,906; William B.Kempler, #28,228; Lawrence J.Bassuk, #29,043 and Gary C.Honeycutt, #20,250

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Gary C. Honeycutt Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265	Gary C. Honeycutt (972) 238-7160

NAME OF INVENTOR: (1)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
Donald C. Abbott	John E. Cotugno	Robert M. Fritzsche
RESIDENCE & POST OFFICE ADDRESS.	RESIDENCE & POST OFFICE ADDRESS:	RESIDENCE & POST OFFICE ADDRESS:
P.O. Box 357, 4 Fernandes Circle Norton, Massachusetts 02766	6 Spring Lane, P.O. Box 496 Little Compton, Rhode Island 02837	61 Reardons Field Lane Attleboro, Massachusetts 02703
COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:
United States	United States	United States
SIGNATURE OF INVENTOR: X Donald C. Abbott	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR: X Robert M Fritzsche
DATE: X March 3, 1999	DATE:	DATE: X March 4, 1999

ATTORNEY'S DOCKET NO.
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APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

TITLE OF INVENTION: Double Sided Flexible Circuit for Integrated Circuit Packages and Method of Manufacture		
NAME OF INVENTOR: (4) Robert A. Sabo	NAME OF INVENTOR: (5) Christopher M. Sullivan	NAME OF INVENTOR: (6) David W. West
RESIDENCE & POST OFFICE ADDRESS: 41 Fenwood Avenue Smithfield, Rhode Island 02904	RESIDENCE & POST OFFICE ADDRESS: 56 Bradford Lane Rochester, Massachusetts 02770	RESIDENCE & POST OFFICE ADDRESS: 59 Barker Street Pembroke, Massachusetts 02359
COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: United States
SIGNATURE OF INVENTOR: X Robert A. Sabo	SIGNATURE OF INVENTOR: X Christopher M. Sullivan	SIGNATURE OF INVENTOR: X David W. West
DATE: X 3/3/99	DATE: X 3/3/99	DATE: X 3/4/99

ATTORNEY'S DOCKET NO.
TI-26904

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Gary C. Honeycutt Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265	Gary C. Honeycutt (972) 238-7160

NAME OF INVENTOR: (1)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
Donald C. Abbott	John E. Cotugno	Robert M. Fritzsche
RESIDENCE & POST OFFICE ADDRESS:	RESIDENCE & POST OFFICE ADDRESS:	RESIDENCE & POST OFFICE ADDRESS:
P.O. Box 357, 4 Fernandes Circle Norton, Massachusetts 02766	6 Spring Lane, P.O. Box 496 Little Compton, Rhode Island 02837	61 Reardons Field Lane Attleboro, Massachusetts 02703
COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:
United States	United States	United States
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR: X	SIGNATURE OF INVENTOR:
DATE:	DATE: X 3/13/99	DATE:

ATTORNEY'S DOCKET NO.
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COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: United States
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE:	DATE:	DATE: